

i860™ 64-BIT MICROPROCESSOR  
PERFORMANCE BRIEF



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PERFORMANCE BRIEF

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#### Revision History:

<u>Date</u>	<u>Release</u>	<u>Changes</u>
2/89	1.0	Original release
8/89	1.1	Linpack measured numbers included
12/89	1.2	Simulated numbers removed
6/90	1.3	SPEC results and measured 40MHz results
8/90	1.4	SPEC results measured 40MHz

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## *The i860 Microprocessor*

The i860 microprocessor is a highly integrated 64-bit RISC microprocessor. It was designed from the ground up to provide the balanced integer and floating point power required for technical and scientific designs such as workstations, servers, and supercomputers. This single chip design contains the basic execution units that perform the high speed computation and the sophisticated 64-bit architecture that sustains this high execution rate. The computational units integrated on-chip are the Integer Execution Unit (IEU), pipelined floating-point adder, pipelined floating-point multiplier and graphics unit.

The on-chip memory interface system includes a 4-KByte instruction cache, 8-KByte data cache and associated paging unit. The on-chip instruction cache can feed the IEU and floating point units 64-bits of instruction each clock cycle. The on-chip data cache bus is 128-bits wide and provides the high speed data path between the cache and the register array required to sustain the high execution rate.

While some degree of execution overlap is common in most microprocessors, the i860 microprocessor is designed to include advanced features supporting multiple instruction issues per clock and up to three operation completions per clock period. The IEU and floating point units can be issued and can execute separate instructions each clock cycle. Furthermore, the floating point instruction

can be a simple scalar floating point instruction or a highly encoded floating point instruction that uses both the pipelined adder and multiplier units.

The efficient 64-bit external data bus is tuned to match the high speed computing data requirements with current DRAM memory capabilities. This efficient bus architecture makes the physical design of second level cache systems easier than multiple chip implementations. Multiple chip implementation forces the hardware designer to pay for the buffer drive time to route signals to an off chip cache. The advantages of a large on-chip cache quickly translates into a more efficient i860 CPU system design for technical workstations. The i860 microprocessor is available today in both 33.3 MHz and 40 MHz speeds.

## *Introduction*

Benchmarks are intended to give a standard measure of performance that can be used to predict how well application code will execute. These benchmark programs should be representative of the intended applications. However, the performance measured is often the combined characteristics of a given computer architecture and many other tightly coupled system software/hardware constituents. Operating system, compilers, libraries, memory design and I/O subsystem characteristic may well dominate the results and make comparisons difficult. This report is intended to show superior i860 Microprocessor performance on standard benchmarks which will translate to superior performance on real applications.

For highest performance, the system software and hardware for the architecture must be finely tuned. This is especially true of a new architecture like the i860 microprocessor. The advanced features of the highly integrated i860 microprocessor design can be exploited at several levels. The first level is to program the i860 microprocessor using only its scalar capabilities. This is the architectural model that ordinary RISC processors have adopted. The second level is to simultaneously issue multiple instructions. The i860 CPU can issue integer instructions and floating point instructions simultaneously and execute them in parallel. The third level is to have the floating point instruction use the full capability of the floating point adder and multiplier pipelines by executing multiple floating point operations in parallel with the integer instruction.

The i860 microprocessor compilers today support single instruction or single floating point operation modes. Compilers that support Dual Instruction Mode and Dual Operation Mode are under development. One performance tool, the Pacific-Sierra Research VAST-2/i860 preprocessor vectorizes FORTRAN DO and IF loops and automatically generates calls to the i860 Vector Primitive Library. The restructuring of code can make a dramatic effect upon performance. As compilers mature and take advantage of proven compiler technology, the power of the i860 architecture available to today's assembly language programmer will be unleashed for the traditional high level language programmer which will immediately translate into increased system performance.

The system used to measure i860 microprocessor performance is a simple, low cost add-in board. The memory subsystem employs a single-bank DRAM design with no external cache. This design introduces excess wait states and hence a performance penalty compared to i860 microprocessor-based workstation designs for memory-access intensive programs like Linpack.

Despite the system suboptimizations, the i860 microprocessor still outperforms other high performance RISC-based workstations and file-servers in the marketplace. The vector processing capability of the i860 microprocessor distinguishes it from other microprocessors, as evidenced by the Linpack results. In fact, the i860 microprocessor approaches supercomputers and mainframes with vector hardware in vector performance. Improvements in compilers, vectorizer, vector libraries, memory subsystem implementation and operating frequency will further increase the system performance of the i860 microprocessor. Possible performance increases from compiler enhancements is evidenced by the increase in Dhrystone 1.1 results since the January 1990 update.

## Performance Summary

### i860 Microprocessor Benchmark Results

Benchmark results for the i860 microprocessor are summarized in Table 1. The benchmarks were executed on the two AT\* add-in board system described in the Test Configuration section. The Intel board uses a 33.3 MHz clock and the Alacron board uses a 40MHz clock.

**Table 1 i860 Microprocessor Benchmark Results**

Benchmarks	33.3 MHz	40 MHz
SPEC (SPECmark)		
Release 1.0	20.6	24.3
Dhrystone (KD/S)		
Version 2.1	68.7	83.1
Version 1.1	94.6	114.0
Dhrystone (MIPS)		
Version 2.1	41.5	50.2
Version 1.1	53.8	64.9
Stanford Integer (MIPS)		
	25.5	29.6
Whetstone (MW/S)		
Single Precision	25.6	31.7
Double Precision	20.0	24.6
Linpack (MFLOPS)		
FORTTRAN Double	4.5	5.4
Coded Double	8.7	10.2

### Performance Comparisons

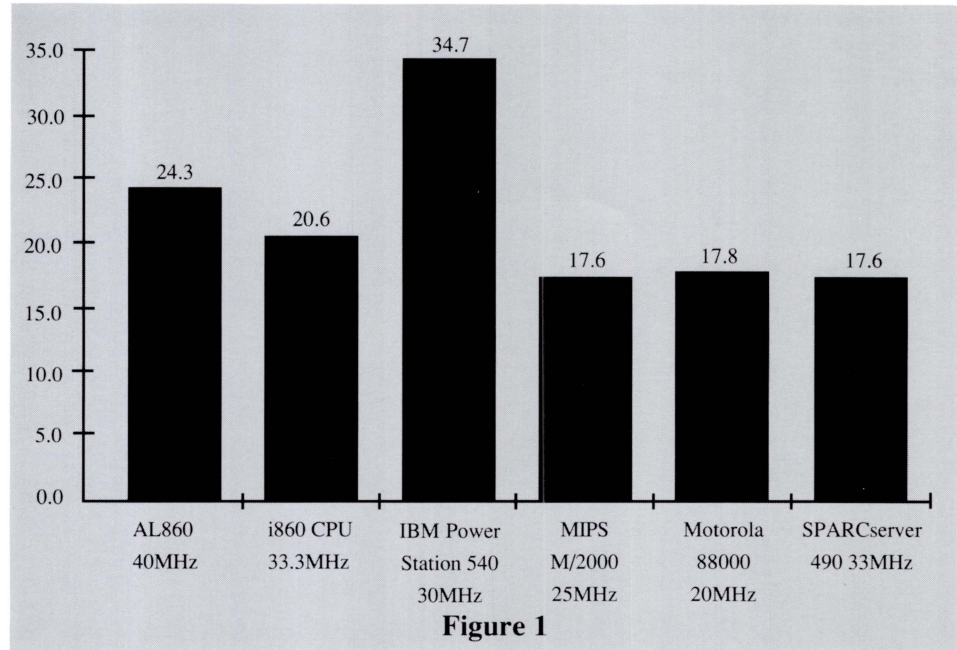
The benchmark results for the i860 microprocessor are compared with results for other microprocessors in Figures 1 through 4. The published performance results are for the fastest available system for each processor. However, not all systems are equally configured. For example, some systems are configured with large amounts of external cache and main memory. In most cases, that will be the IBM\* Power Station 540 file server, MIPS M/2000 file server, SPARCserver 490 and Motorola Delta Series Model 8612. Not all of the results reported here are from the fastest processor speed available for

a specific manufacturer on all of the different benchmarks. In these cases, the best results available at this time are reported. The data on the MIPS R3000, Motorola 88000 and Sun SPARC are published data [SPEC 89][MIPS 89], [SUN 89]

and [IBM 90].

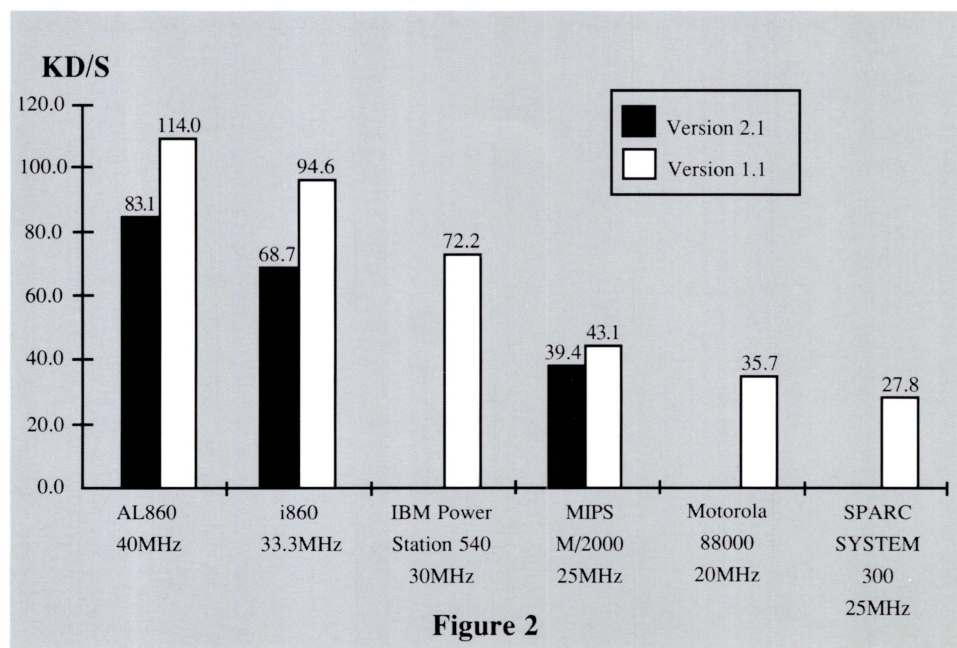
Because other vendor processor implementations may not scale linearly with the frequency, prediction of their performance results at higher frequencies by extrapolating is avoided.

**SPEC Benchmark**



**Figure 1**

**Dhrystone Benchmark**



**Figure 2**

As illustrated in the comparisons, a simple DRAM-only i860 microprocessor-based system like the add-in boards used outperform most commercial RISC-based systems that are considerably more

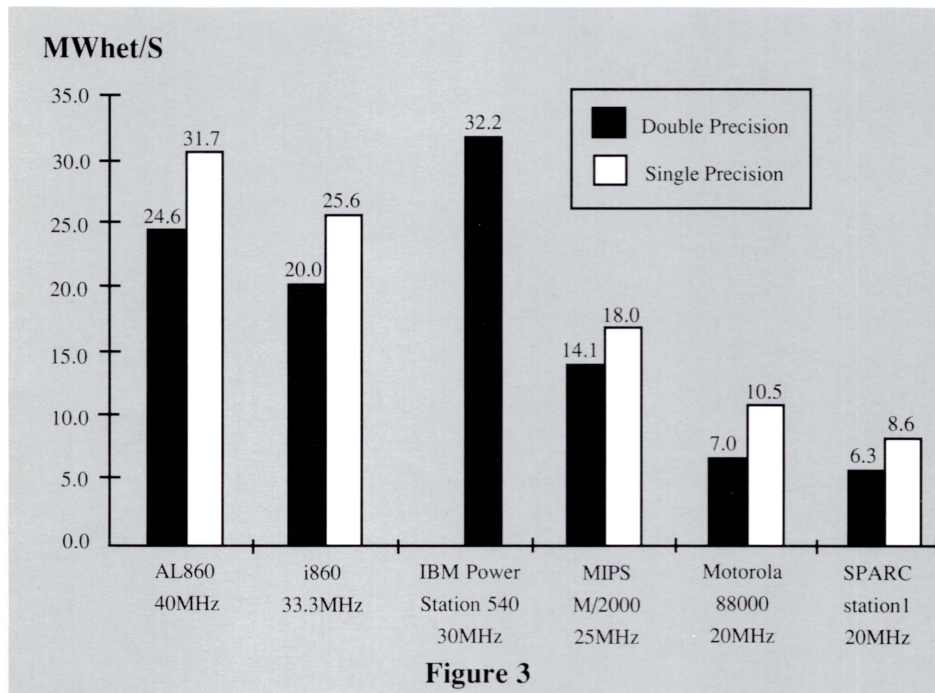
expensive. Those RISC systems are more optimized in hardware and software. The i860 CPU system performance lead will widen further as hardware and software designs are optimized.

## Choice of Benchmarks

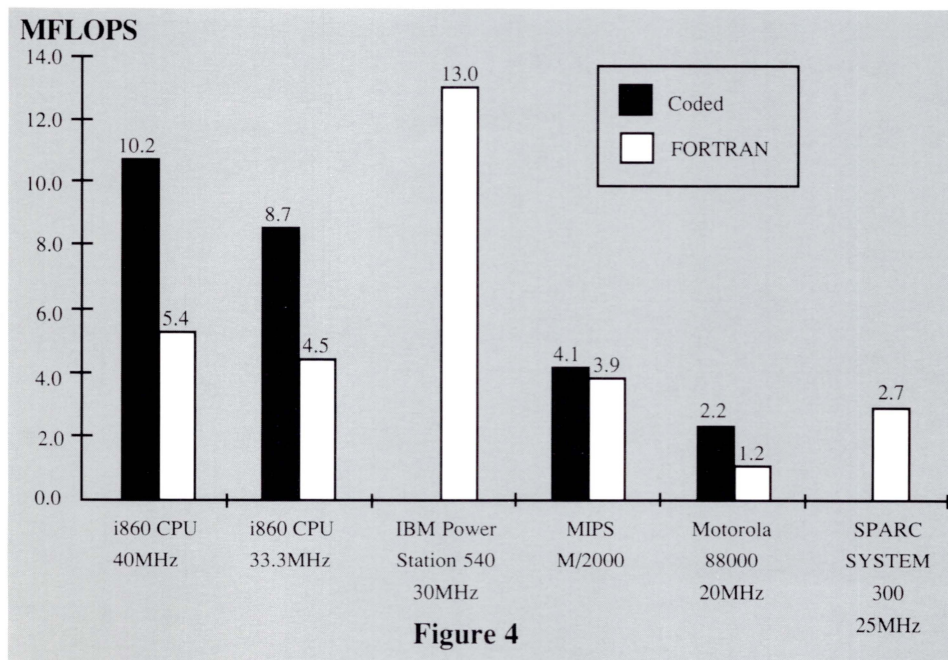
The System Performance Evaluation Cooperative (SPEC) was formed by a group of leading computer companies to develop a benchmark suite that better represent all aspects of computer performance than today's popular benchmarks. SPEC Benchmark Suite Release 1.0 is the first release from SPEC. Since the release, the SPEC Benchmark Suite has rapidly gained popularity and is often the first performance indicator requested especially in the workstation market. SPEC Release 1.0 focuses on a mix of ten compute intensive actual applications that provide a good indicator for system comparisons. The SPEC Benchmark Suite is written in both C and FORTRAN and measures scalar, floating-point, and vector performance.

Other well accepted "industry standard" benchmarks used are Dhrystone and Stanford Integer Suite to evaluate integer performance and Whetstone and Linpack to evaluate floating-point performance. Both version 2.1 and 1.1 of Dhrystone are used.

**Whetstone Benchmark**



**Linpack (Double Precision)**



## *i860 Microprocessor Test Configurations*

The benchmarks were executed with the following hardware/software configurations and conditions.

### **Measured Systems**

---

#### **i860 Microprocessor-based Add-in Board from Intel**

- 33.3MHz i860 microprocessor, with 4-KByte instruction cache and 8-KByte data cache
- No external second level cache
- 8 MBytes of static column DRAMs, organized in a single bank configuration
- DRAM-only memory design
  - zero wait state for consecutive “NExt-NEar” reads or writes within the same DRAM row
  - eight wait states for read if CPU idle bus states occur between “NExt-NEar” bus cycles
  - five wait states for writes if CPU idle bus states occur between “NExt-NEar” bus cycles
  - five wait states for reads from idle
  - two wait states for writes from idle
- Intel STAR860 Development system host and APX software

#### **AL860 Accelerator Add-in Board from Alacron:**

- 40MHz i860 microprocessor, with 4-KByte instruction cache and 8-KByte data cache
- No external second level cache
- 8 MBytes of fast page mode DRAMs, organized in a single bank configuration
- DRAM-only memory design
  - zero wait states for consecutive “NExt-NEar” reads or writes within the same DRAM row
  - zero wait states for write after read “NExt-NEar” bus cycles
  - two wait states for read after write “NExt-NEar” bus cycles
  - five wait states for far access
  - five wait states for an access from idle
  - quad port memory design with i860 microprocessor the idle owner and lowest priority in arbitration.
- Intel STAR860 Development system host, APX software tools, and Alacron rt860 run time environment

Contact Alacron for more details on the AL860 Accelerator at:

Alacron Inc.  
Suite 349, 980 Broadway,  
Thornwood, NY 10594  
Telephone (914) 948-3145

## Compilation and Run-Time Conditions

**Software:** *The Application Processor Executive (APX) Release 5.0* software connects the measured i860 microprocessor based add-in board to the 386 microprocessor-based host machine. The APX software resides on both the host and the i860 microprocessor-based add-in board. It provides the system call resources for i860 microprocessor application code via UNIX/386 system calls. The compilers, linker, assembler and most other software tools execute on the i860 microprocessor add-in board.

The host STAR860 system is running UNIX/386 System V Rel. 3.2 in multi-user mode. Standard UNIX demons are running and a single user is logged on. The AL860 Accelerator Board uses the same host system and a UNIX interface driver and environment designed by Alacron.

## Compilers:

Benchmark	Compiler Version	Compiler options
SPEC	Metaware High C R2.1f Green Hills Fortran 1.8.5 R5.0 Pacific-Sierra Research VAST-2 2.25.3	-O -sched -Hi -bigalign -OLM
Dhrystone1.1	Metaware High C R2.1f	-O-sched -Hi -bigalign
Dhrystone2.1	Green Hills C 1.8.5	-OLM
Stanford	Green Hills C 1.8.5	-OLM
Whetstone	Green Hills Fortran 1.8.5 R4.1	-OLM
Linpack	Green Hills Fortran 1.8.5 R5.0 Pacific-Sierra Research VAST-2 2.25.3	-OLM

Refer to compiler documents provided by the compiler vendors for option explanation

**Vectorizer:** The Pacific-Sierra Research Fortran vectorizer (version 2.25.3) functions as a preprocessor for vectorizing code. An equivalent Fortran program containing calls to vector libraries is produced. The vectorizer was used to optimize Linpack, SPEC 020.nasa7, SPEC 030.matrix300, and SPEC 047.tomcatv prior to FORTRAN compilation.

**Libraries:** Intel vector library (version 2.25.3) and Intel's scalar math library (version1.1) were used.

## Timing Measurements and APX Software Interrupt Overhead

On the Intel board the timing mechanism is implemented via 75 Hz timer. Interrupts to the i860 microprocessor occur every 13.3 milliseconds. Interrupt overhead in the APX software cannot be singled out and hence is included in the results. As much as 4% performance degradation due to the interrupt overhead has been identified in benchmarks. A similar timing mechanism is used on the Alacron board with a 100 Hz timer. The Stanford Integer Suite executes too quickly to accurately measure with a 13.3 milliseconds timer, so the timer was set down to 6.67 milliseconds for Stanford Integer Suite.

The SPEC Benchmarks use the UNIX system function /bin/time to time each of the 10 benchmarks. As a result the time required to load the benchmark is included in the result. This is a disadvantage for the add-in boards with slower I/O systems. A one to eight per cent performance increase on the different SPEC benchmarks can be expected on a UNIX/860 based system with a well designed I/O system.

## Benchmark Results

The benchmark results are discussed below. A brief description of each benchmark is also given. Performance numbers for other microprocessors are published data [SPEC 90, MIPS 89, SUN 89].

### SPEC

The SPEC Benchmark Suite Release 1.0 consists of 6 Fortran and 4 C benchmarks that are intended to be meaningful samples of applications which perform fixed-point, floating-point, logical, and arithmetic operations in a technical computing environment.

The SPEC Benchmark Suite Release 1.0 benchmarks have been derived from publicly-available application programs. The GNU C compiler benchmark exhibits a moderate amount of I/O. The remaining nine benchmarks exhibit little or no I/O. All of the SPEC Benchmark were executed in accordance with the SPEC reporting rules. Portability changes were required for GNU C and Eqntott. A brief explanation of each benchmark used in our tests follows.

### GNU C Compiler

The GNU C Compiler (GCC) benchmark is a CPU-intensive, integer-intensive benchmark. The GNU C Compiler benchmark measures elapsed time and not CPU time. It is based on the GNU C compiler, version 1.35, distributed by the Free Software Foundation. The APX environment does not support the UNIX function “fork”, so the GCC compiler was executed with a shell script.

Minor portability changes were required to make the GCC source code conform to ANSI standard syntax.

### Espresso

Espresso is an application program used as a design tool in generation and optimization of programmable logic arrays. It is an integer-intensive application and as a result provides information on the capabilities of the system as a logic simulator or when used in applications such as routing algorithms.

### Spice2G6

Spice is an analog circuit-simulation package which performs most of its heavy number-crunching in double-precision floating-point. It is considered to be a real application as opposed to a synthetic benchmark and therefore is a very good representation of the system’s capabilities as an EDA platform.

### Doduc

Doduc is a Monte Carlo simulation of the time evolution of a thermohydraulic model of a nuclear reactor component. It performs many short branches and loops and uses 64-bit floating-point numbers. It is popular in segments of the physics community.

### Nasa7

Nasa7 stands for the seven modules in the NASA Ames Kernel benchmark. It is a collection of floating-point intensive matrix computations. These computations are highly parallel in nature and benefit from vectorization.

### Li

Li is a Lisp interpreter and it measures the time required to solve the 9-queens problem. It is a CPU-

intensive integer benchmark.

### Eqntott

Eqntott is an integer-intensive benchmark written in C whose primary task is sorting. It translates a logical representation of a Boolean equation into a truth table. It uses dynamic memory allocation. The APX environment does not support the UNIX function “fork”, so the “fork” process that executes the pre-processor was removed. The effect on performance was not measurable with the /bin/time timer accuracy on a UNIX/386 system and is assumed to be negligible on the i860 micro-processor also.

### Matrix300

Matrix300 is a vectorizable Fortran scientific benchmark that performs matrix operations. It measures the time elapsed between two internally defined points within the benchmark.

### Fppppp

Fppppp is a quantum chemistry floating-point-intensive benchmark that measures performance on a two-electron integral derivative computation.

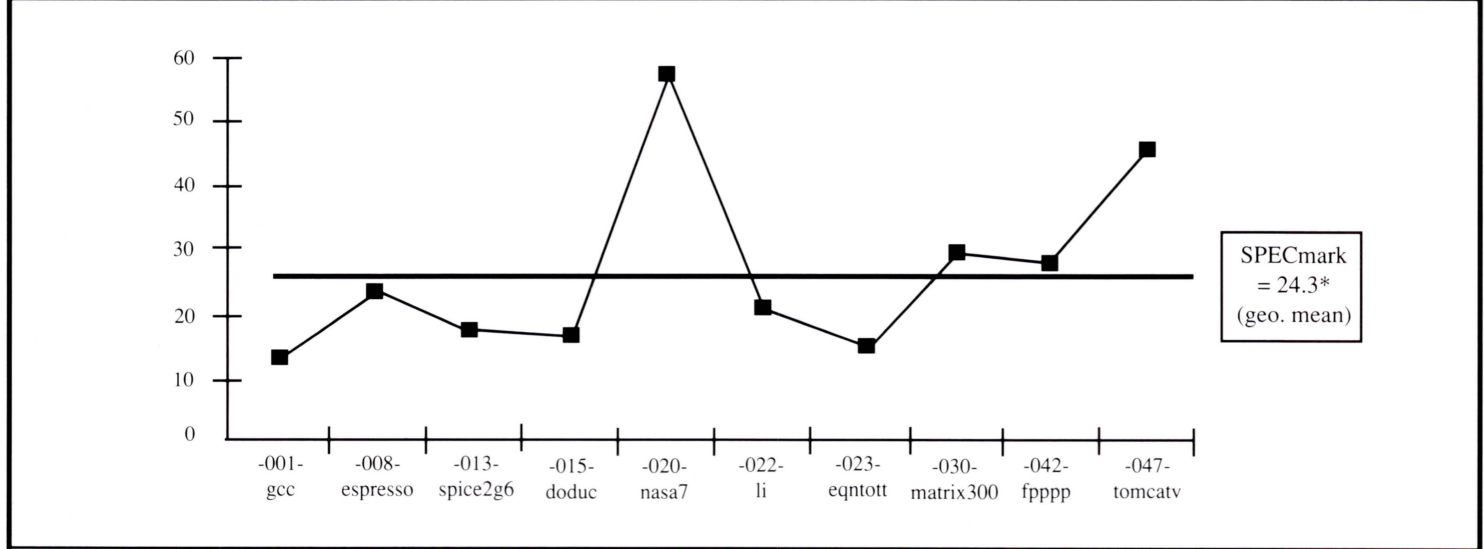
### Tomcatv

Tomcatv is a vectorizable floating-point Fortran benchmark that does little I/O. It was originally intended to measure the actual computation time, not including program load and initialization code execution.

# SPEC Benchmark Release 1.0 Summary

RESULTS Benchmark No. & Name	SPEC		AL860 Accelerator		Alacron Inc. AL860 Accelerator
	Reference Time (seconds)		Time (seconds)	SPEC Ratio	
001. gcc*	1482		100*	14.8*	<b>Hardware</b> Model Number: AL860 Accel., 386/25AT host CPU: i860 40MHz FPU: Integrated Number of CPUs: 1 Cache Size Per CPU: Integrated 8KB data/4KB instruc. Memory: 16MB Disk Subsystem: 179MB SCSI Winchester Other Hardware: 60MB SCSI Tape/Floppy  <b>Software</b> O/S Type and Rev: UNIX386 Sys V R3.2, APX R5 AL860 runtime from Alacron <sup>(1)</sup> C Compiler Rev: Metaware Hi C 2.1f FORTRAN Compiler Rev: Green Hills 1.8.5 PSR VAST-2 V 2.25  <b>System</b> Tuning Parameters: None in use Background Load: None System State: Single-user log-on
008. espresso*	2266		105*	21.6*	
013. spice 2g6	23951		1320	18.1	
015. doduc	1863		109	17.1	
020. nasa7	20093		351	57.2	
022. li*	6206		286*	21.7*	
023. eqntott*	1101		60*	18.4*	
030. matrix300	4525		161	28.1	
042. fpppp	3038		117	26.0	
047. tomcatv	2649		61	43.4	
Geometric Mean				24.3*	<b>General Availability: Now</b>

Tested in: May 1990	By: Intel Corp.	Of: Santa Clara, CA	SPEC License # 014
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**Notes/Summary of Changes** (\*portability changes to the benchmarks)

- \* gcc: 1.35 has numerous changes to bring it to ANSI C compliance. See note <sup>(1)</sup> below.
- \* espresso: has one change of stdlib consistency.
- \* li: has one change to convert "vararg" to "stdarg".
- \* eqntott: See note <sup>(1)</sup> below.

<sup>(1)</sup> The Alacron runtime environment does not support "fork", therefore: gcc 1.35 executes "cc1" from a shell script; and, eqntott has the fork call to the preprocessor commented out. 0.1 seconds (the time for an i386 CPU to execute the preprocessor) has been added to the time to compensate.

## SPEC Benchmark Release 1.0 Summary

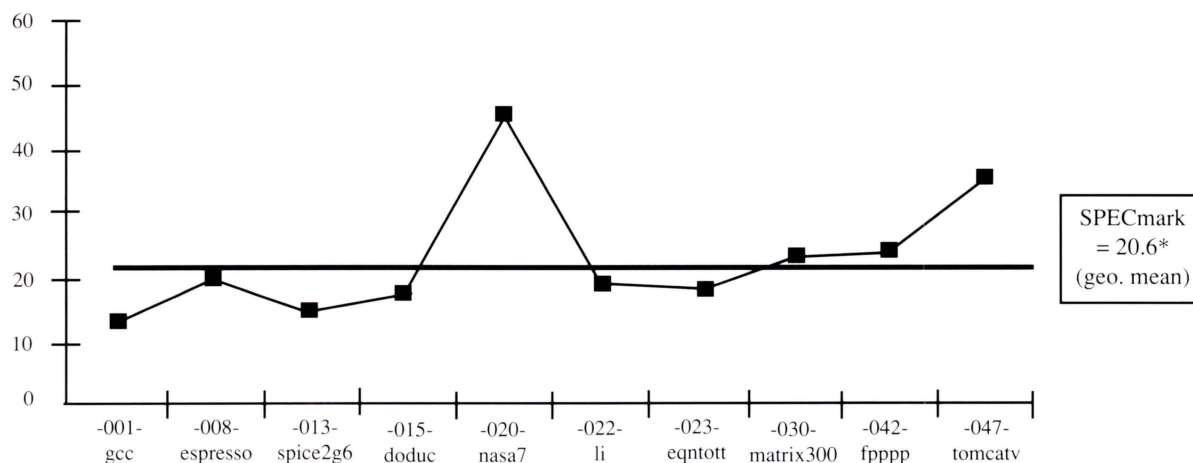
RESULTS Benchmark No. & Name	SPEC		Intel Corp. STAR860	Intel Corp. STAR860
	Reference Time (seconds)	Time (seconds)	SPEC Ratio	
001. gcc*	1482	119.8*	12.4*	<b>Hardware</b> Model Number: STAR860 CPU: i860 CPU 33.3MHz FPU: Integrated Number of CPUs: 1 Cache Size Per CPU: Integrated 8KB data/4KB instruc. Memory: 8MB Disk Subsystem: 179MB SCSI Winchester Other Hardware: 60MB SCSI Tape/Floppy  <b>Software</b> O/S Type and Rev: UNIX386 Sys V R3.2 APX 1.2 R5 <sup>(1)</sup> C Compiler Rev: Metaware Hi C 2.1f FORTRAN Compiler Rev: Green Hills 1.8.5/ PSR VAST-2 V 2.25  <b>System</b> Tuning Parameters: None in use Background Load: None System State: Single-user log-on
008. espresso*	2266	113.1*	20.0*	
013. spice 2g6	23951	1620.0	14.8	
015. doduc	1863	119.5	15.6	
020. nasa7	20093	446.8	45.0	
022. li*	6206	350.0*	17.7*	
023. eqntott*	1101	62.0*	17.8*	
030. matrix300	4525	210.9	21.5	
042. fpppp	3038	139.6	21.8	
047. tomcatv	2649	74.0	35.8	
Geometric Mean			20.6*	<b>General Availability: Now</b>

Tested in: May 1990

By: Intel Corp.

Of: Santa Clara, CA

SPEC License # 014



### Notes/Summary of Changes (\*portability changes to the benchmarks)

- \* gcc: 1.35 has numerous changes to bring it to ANSI C compatible. See note <sup>(1)</sup> below. None of the changes affect performance.
- \* espresso: has one change of stdlib consistency.
- \* li: has one change to convert "vararg" to "stdarg".
- \* eqntott: See note<sup>(1)</sup> below.

<sup>(1)</sup> The APX environment does not support "fork", therefore: gcc 1.35 executes "cc1" from a shell script; and, eqntott has the fork call to the preprocessor commented out. 0.1 seconds (the time for an i386 CPU to execute the preprocessor) has been added to the time to compensate.

Table 2 SPEC Benchmark (rel. 1.0) Summary

Gcc	Espresso	Spice2G6	Doduc	Nasa7	Li	Eqntott	Matrix300	Fpppp	Tomcatv	Specmark	System
7.6	8.9	7.0	8.3	9.7	9.7	8.8	7.2	8.9	7.3	8.3	DECstation 2100
13.8	12.2	8.8	5.8	5.8	16.8	11.0	9.5	7.0	4.3	8.7	Intel i486 CPU at 25MHz
9.6	12.8	8.2	6.7	8.9	12.9	10.3	10.3	8.0	8.0	9.4	Data General AV 410
8.6	11.8	9.0	9.9	13.3	14.2	11.5	9.6	4.9	11.0	10.0	MIPS RC2030
10.9	12.0	9.5	11.3	13.2	13.1	11.2	9.8	12.5	9.9	11.3	DECstation 3100
11.0	14.1	9.1	12.8	12.8	12.2	13.6	10.4	13.4	9.9	11.8	DECsystem 5400
13.8	11.6	11.4	9.5	14.0	11.2	12.6	14.7	13.1	8.2	11.8	Sun SPARCstation 330
13.4	13.9	10.6	11.1	12.6	15.5	13.3	9.9	12.2	10.7	12.2	CDC 920B-450
13.4	13.9	10.6	11.1	12.6	15.5	13.3	9.9	12.2	10.7	12.2	Silicon Graphics 4D/25S
18.1	16.7	10.0	14.7	14.4	16.3	16.2	9.7	16.1	10.8	14.0	CDC 910B-621
18.1	16.7	10.0	14.7	14.4	16.3	16.2	9.7	16.1	10.8	14.0	Silicon Graphics 4D/210S
15.3	17.3	13.6	15.8	18.1	20.3	17.2	13.6	17.5	14.2	16.2	CDC 4340
12.8	12.9	11.9	23.0	20.5	11.1	11.1	22.0	32.0	19.9	16.6	HP Apollo Series 10000
19.2	18.0	13.5	17.1	18.4	23.9	18.4	13.3	20.0	16.9	17.6	CDC 4360
19.0	18.3	12.1	17.6	18.4	23.8	18.4	13.3	20.4	17.7	17.6	MIPS M/2000
18.8	18.1	13.5	17.4	18.4	23.9	18.4	13.4	20.1	17.1	17.7	CDC 4380
18.3	23.0	14.8	12.2	17.5	23.9	20.7	21.5	15.3	14.9	17.8	Motorola Delta Series Model 8612
17.3	18.5	13.7	18.2	22.6	21.8	18.4	17.0	22.0	17.3	18.5	DECstation 5000 200
<b>12.4</b>	<b>20.0</b>	<b>14.8</b>	<b>15.6</b>	<b>45.0</b>	<b>17.7</b>	<b>17.8</b>	<b>21.5</b>	<b>21.8</b>	<b>35.8</b>	<b>20.6</b>	<b>Intel i860 <math>\mu</math>P board at 33.3MHz</b>
13.7	16.3	19.8	21.6	26.6	15.6	17.7	17.5	42.9	56.5	22.3	IBM RISC System/6000 320
<b>14.8</b>	<b>21.6</b>	<b>18.1</b>	<b>17.1</b>	<b>57.2</b>	<b>21.7</b>	<b>18.4</b>	<b>28.1</b>	<b>26.0</b>	<b>43.4</b>	<b>24.3</b>	<b>AL860 Accelerator at 40MHz</b>
17.8	20.7	27.6	27.7	35.5	19.8	23.0	21.8	54.7	75.7	28.9	IBM RISC System/6000 530
17.8	20.3	14.7	19.7	62.9	18.1	18.2	108.5	29.1	61.9	29.0	Stardent Computer Stardent 3010
21.0	24.9	33.2	33.1	43.4	23.7	26.7	26.5	65.8	91.0	34.7	IBM RISC System/6000 540
44.5	43.7	37.7	38.3	39.6	44.9	35.6	52.4	52.2	36.8	42.2	MIPS RC6280, 60MHz Beta

Source: Intel, [SPEC 90]

## Dhrystone

Dhrystone was developed in ADA by R. Weicker in 1984. C versions of the benchmark are more commonly used. It is a synthetic integer benchmark with its instruction profile based on program analysis. Language constructs used in typical programs in a variety of languages were analyzed. The benchmark includes weighted percentages of procedural calls, loops, integer assignments, integer arithmetic and logical operations. It is designed to measure system programming performance. Therefore, it evaluates not only microprocessor performance but also compiler efficiency. The result is expressed in Dhrystones/second (D/S). The Dhrystone test was executed with a loop count of 1,000,000 and timed using the 6.6 millisecond timer on the i860 microprocessor card.

When Dhrystone results are quoted without additional qualifications, they are obtained with the REGS attribute for interprocedural register allocation. Some vendors quote a MIPS performance rating for their processor by dividing Dhrystone version results by results obtained on the VAX 11/780. By this measure, the 40 MHz i860 microprocessor becomes a 50.2 MIPS CPU for Version 2.1. This result is provided here for comparison with similar measurements published.

Version 2.1 results are more desirable than the Version 1.1 results. Many benchmark reports provide results using Version 1.1. Version 2.1 includes modifications designed to defeat code suppression by optimizing compilers. Both results have been included here for comparison.

The i860 microprocessor performs 68.7 KD/S at 33.3 MHz and 83.1KD/S at 40MHz for Version 2.1 and 94.6 KD/S at 33.3 MHz and 114.0 K D/S at 40 MHz for Version 1.1. Single cycle test and branch, 128-bit loads and other unique architecture features contribute to

the high performance.

Listed in Tables 3 and 4 are the results of versions 2.1 and 1.1 respectively of Dhrystone for the i860 microprocessor and the published data for other microprocessors and their comparable MIPS rating.

**Table 3 Dhrystone (ver. 2.1) Benchmark Results**

D/S	Rel.	Systems
1,657	1.0	DEC VAX 11/780, 4.3 BSD cc [MIPS 88]
1,784	1.1	DEC VAX 11/780 4.3 BSD gcc [MIPS 89]
22,400	13.5	DECstation 3100 cc 1.31
24,700	14.9	MIPS M/12-5 cc 1.31
25,500	15.4	MIPS M/120-5 cc 2.0 RISC/OS 3.10
25,600	15.4	MIPS RC2030 cc 2.0 RISC/OS 3.10
31,989	19.3	Intel i486 CPU at 25MHz, hand coded stremp
33,296	20.1	Motorola Sys8600, 20MHz 88000 [Mot 89]
38,800	23.4	MIPS M/2000-8 cc 1.31
39,400	23.8	MIPS M/2000-8 cc 2.0
<b>68,700</b>	<b>41.5</b>	<b>Intel i860 <math>\mu</math> P board at 33.3MHz</b>
<b>83,100</b>	<b>50.2</b>	<b>AL860 Accelerator 40MHz</b>

Source: Intel, [MIPS 89], [SUN 89]

**Table 4 Dhrystone (ver. 1.1) Benchmark Results**

D/S	Rel.	Systems
1,571	0.9	VAX 11/780, 4.3BSD, f77 [MIPS 88]
1,757	1.0	VAX 11/780 VAX/VMS 4.2 [Intergraph 86]
3,850	2.2	Sun-3/100 [Muchnick 88]
6,374	3.6	Sun-3/260, 25MHz 68020 SunOS 3.2
6,423	3.7	VAX 8600, 4.3BSD
6,440	3.7	IBM 4381-2, UTS V, cc 1.11 IBM 4381-2, UTS V, cc 1.11
6,896	3.9	Intergraph InterPro-32C SYSV R3 3.0.0, Greenhills, -O
7,109	4.0	Apollo DN4000, -O
7,140	4.1	Sun-3/200 [Muchnick 88]
7,249	4.2	Convex C-1 XP 6.0, vc 1.1
7,409	4.2	VAX 8600, VAX/VMS in [Intergraph 86]
7,655	4.4	Alliant FX/8 [Alliant 86]
8,309	4.7	InterPro-326, 30MHz Clipper, Greenhills [Intergraph 86]
9,436	5.4	Convergent Server PC, 20MHz, 80386, Greenhills
9,920	5.6	HP 9000/840S [HP 87]
10,416	5.9	VAX 8550, VAX/VMS 4.5, cc 2.2
10,787	6.1	VAX 8650, VAX/VMS [Intergraph 86]
11,215	6.4	HP 9000/840, HP-UX, full optimization
12,639	7.2	HP 9000/825S [HP 87]
13,000	7.4	MIPS M/500, 8MHz R2000, -O3
13,157	7.5	HP 825SRX [Sun 87]
14,109	8.0	Sun-4/110 [Sun 88]
14,195	8.1	Multiflow Trace 7/200 [Multiflow]
14,820	8.4	CRAY 1S
15,007	8.5	IBM 3081, UTS SUR2.5, cc 1.5
15,576	8.9	HP 9000/850 [HP87]
18,530	10.5	Cray X-MP
19,000	10.8	Sun-4/200, 16.7MHz SPARC [Muchnick 88], -O3
19,800	11.3	MIPS M/800, 12.5MHz R200, -O3
22,049	12.5	Sun SPARCstation 1 [Sun 89]
23,430	13.3	HP 835S [RISC Mgmt, 88]
23,700	13.5	MIPS M/1000, 15MHz R2000, -O3
25,000	14.2	DECstation 3100
25,461	14.5	Apollo DN10000 [Apollo 88]
27,400	15.6	MIPS M/120-5, 16.7MHz R2000, -O3
27,777	15.8	Sun SPARCsystem 300, SunOS 4.0.3 [Sun 84]
28,846	16.4	Amdahl 5860, UTS-V, cc1.22
31,250	17.8	IBM 3090/200
35,285	20.1	Intel i486 CPU at 25MHz, hand coded strcmp
35,653	20.3	AMD 2900, 25MHz, 2 8K caches (simulation) [AMD 88]
35,714	20.3	Motorola 88000, 20MHz [MIPS 89]
43,100	24.5	MIPS M/2000, 25MHz R3000, -O3 cc 2.0
43,668	24.9	Amdahl 5890/300E, cc-O
48,300	27.5	IBM Power Station 320
53,108	30.2	CCI Power 7/64 (simulation) [Simpson 88]
60,700	34.5	IBM Power Station 530
72,200	41.1	IBM Power Station 540
<b>94,557</b>	<b>53.8</b>	<b>Intel i860 <math>\mu</math> P board at 33.3MHz</b>
<b>114,025</b>	<b>64.9</b>	<b>AL860 Accelerator at 40MHz</b>

Source: Intel, [MIPS 89], [SUN 89]

### Stanford Integer Suite

The Stanford Integer Suite is a collection of programs which are small both in terms of size and execution time. They were originated from the Computer Systems Lab at Stanford University. They are samples of code chosen from various applications. The limitations are in their relatively small program size and short execution time. The results are measured in seconds; however,

VAX MIPS numbers are derived by comparing timings to the VAX 11/780.

The high speed of the i860 microprocessor has made the measurement of short execution times very imprecise given the crude timing mechanism implemented on the measured system. As much as 16-20% error in some modules in the suite has been identified. With the timer period of 13.3 milliseconds,

the tests take from 2 to 16 clock ticks to complete. Therefore, the timer period was changed to 6.7 milliseconds for this benchmark to improve the accuracy of the measurement. The measured numbers are included here for completeness. Listed in Table 5 are the Stanford Integer Suite results for the i860 microprocessor and the published data for other microprocessors [MIPS 89].

**Table 5 Stanford Integer Suite Benchmark Results**

Perm (Sec)	Tower (Sec)	Queen (Sec)	Intmm (Sec)	Puzzle (Sec)	Quick (Sec)	Bubble (Sec)	Tree (Sec)	Geo Mean	Rel. Perf	Systems
2.34	2.30	.94	1.67	11.23	1.12	1.51	2.72	2.14	.7	VAX 11/788 4.3BSD
								1.60	1.0	VAX 11/180 est. [MIPS 88]
.63	.63	.27	.73	2.96	.31	.44	.69	.62	2.6	VAX 8600 Ultrix 1.2
.75	.95	.30	.40	1.82	.34	.39	1.24	.53	3.0	Sun-3/100
.41	.48	.18	.25	1.09	.20	.23	.70	.36	4.4	Sun-3/200-03
.28	.35	.17	.42	2.22	.18	.25	.35	.35	4.6	VAX 8550 Ultrix 2.0 cc-0
.28	.35	.13	.15	.88	.13	.17	.50	.26	6.2	VAX 8550 Ultrix 2.0 vcc-0
.18	.24	.15	.23	1.15	.17	.19	.34	.26	6.2	MIPS M/500
								.22	7.3	Sun-4/110 [Sun 88]
.12	.16	.11	.13	.61	.10	.12	.22	.16	10.0	MIPS M/500
.11	.17	.09	.15	.55	.10	.12	.20	.15	10.7	Sun-4/200, 16.7MHz SPARC
.097	.124	.067	.135	.694	.089	.124	.142	.136	11.8	29K+VRAM, 25MHz [AMD 88]
.10	.13	.10	.11	.51	.08	.10	.17	.13	12.3	MIPS M/1000
.097	.118	.077	.089	.458	.072	.092	.164	.118	13.3	MIPS M/120-5
.116	.13	.091	.088	.48	.071	.092	.154	.115	13.9	DECstation 3100
.066	.096	.052	.120	.559	.077	.089	.130	.109	14.7	29K cache, 25MHz [AMD 88]
.065	.078	.045	.059	.303	.048	.060	.108	.075	21.3	M/2000-8, 25MHz R3000 cc1.31
<b>.060</b>	<b>.073</b>	<b>.040</b>	<b>.033</b>	<b>.207</b>	<b>.040</b>	<b>.053</b>	<b>.093</b>	<b>.063</b>	<b>25.5</b>	<b>Intel i860 <math>\mu</math> P at 33.3MHz</b>
<b>.050</b>	<b>.060</b>	<b>.040</b>	<b>.030</b>	<b>.170</b>	<b>.030</b>	<b>.050</b>	<b>.080</b>	<b>.054</b>	<b>29.6</b>	<b>AL860 Accelerator at 40MHz</b>

Source: Intel [MIPS 89] [SUN 89]

## Whetstone

The Whetstone benchmark was developed in the late 1960's by Curnow and Wichman at the National Physical Laboratory in Whetstone, England. It was designed to predict the performance in a floating-point intensive environment. The benchmark is a synthetic mix of floating-point and integer arithmetic, transcendental functions, floating-point array computations, and subroutine calls. It is based on statistics on scientific Fortran programs. The size of the measurement is rather small and hence fits in the cache for most systems. It is a popular workstation benchmark. The result is measured in Whetstone Instructions/second (MW/S) and is usually reposted as thousands of Whetstones per second (KW/S) or in millions of Whetstones per second. Whetstone code is not vectorizable and hence evaluates scalar performance.

The single-precision and double-precision results obtained on the measured 33.3 MHz system are 25.6 MW/S and 20.0 MW/S. Measured results on the 40 MHz system are 31.7 MW/S and 24.6 MW/S. The i860 microprocessor again delivers higher scalar performance than other microprocessors. Improvements in the performance are expected with future release of the compilers and libraries. Listed in Table 6 are Whetstone benchmark results for the i860 microprocessor and the published data for other microprocessors.

**Table 6 Whetstone Benchmark Results Table**

DP (Kwips)	SP (Kwips)	Systems
410	500	VAX 11/780, 4.3BSD, f77 [MIPS 88]
715	1,893	VAX 11/780, LLL compiler [MIPS 88]
830	1,250	VAX 11/780 VAX/VMS [Intergraph 86]
924	1,039	Sun-3/160C. 68881 [Wilson 88]
1,230	1,250	Sun-3/260, 25MHz 68020, 20MHz 68881
1,581	1,886	Apollo DN4000, 25MHz 68020, 25MHz 68881 [Wilson 88]
1,730	1,860	Intel 80386+80387, 20MHz, 64K cache, Greenhills
1,740	2,980	Intergraph InterPro-32C 30MHz Clipper [Intergraph 86]
1,863	2,433	Sun-3/260, 25MHz 68020, 20MHz 68881
2,092	3,115	HP 9000/840S [HP 87]
2,433	3,521	HP 9000/825S [HP 87]
2,590	4,170	Intel 80386+Weitek 1167, 20MHz, Greenhill
2,673	3,569	Sun-3/260, Weitek FPA [Wilson 88]
2,670	4,590	VAX 8600, VAX/VMS [Intergraph 86]
2,907	4,202	HP 9000/850S [HP 87]
2,940	4,215	Sun-4/110 [Sun 88]
3,885	5,663	Sun-4/200, 16.7MHz SPARC, Wietek 1164/5 [Wilson 88]
3,950	6,670	VAX 8700, VAX/VMS, Pascal(?) [McInnis 87]
4,000	6,900	VAX 8650, VAX/VMS [Intergraph 86]
4,120	4,930	Alliant FX/8 (1CE) [Alliant 86]
4,200	-	Convex C-1 XP [Multiflow]
4,220	5,430	MIPS M/500
5,637	5,903	Intel i486 25MHz
6,600	-	HP 835S [RISC Mgmt, 88]
6,930	8,570	MIPS M/800
7,000	10,500	Motorola 20MHz 88000 [MIPS 89]
7,960	10,280	MIPS M/1000
8,820	11,500	DECstation 3100, f77 1.31, -03
9,100	11,400	MIPS M/120-5
12,605	-	Multiflow Trace 7/200 [Multiflow]
14,100	18,000	MIPS M/2000-8, 25MHz R3000/R3010, f77 s.0
14,069	-	CCI Power 7/64 (simulation) [Simpson 88]
14,924	16,969	Apollo DN10000 [Apollo 88]
<b>20,000</b>	<b>25,641</b>	<b>Intel i860 <math>\mu</math> P board at 33.3MHz</b>
<b>24,600</b>	<b>31,700</b>	<b>AI860 Accelerator at 40MHz</b>
25,000	-	IBM 3090-200 [Multiflow]
35,000	-	Cray X-MP/12

Source: Intel, [MIPS 89], [SUN 89]

## Linpack

Linpack is a collection of Fortran subroutines which analyze and solve simultaneous linear algebraic equations. The benchmark is highly floating-point computation intensive. It was originally designed by Jack Dongarra, et al, of the Argonne National Laboratories in 1978. The intent was to give users of the Linpack software package information on execution time on solving a sample system of linear equations. Since arrays are the primary data structures, the benchmark can be vectorized. As a result, it is often used to benchmark in supercomputing or vector processing environments. The benchmark result is expressed in MFLOPS (millions of floating-point operations per second).

Most of the floating-point operations take place in the subroutine, DAXPY (for double precision; SAXPY for single precision) which is part of the Basic Linear Algebra Subprograms (BLAS) in the Linpack software package. The subroutine is repeatedly called by two major timing routines, DGEFA and DGESL (for double precision; SGEFA and SGESL for single precision) which perform standard LU decomposition with partial pivoting and back-substitution. Although  $100 \times 100$  matrix calculations are to be performed, the inner loop references the arrays in the one-dimensional form,  $y[i] = y[i] + a * x[i]$ . All calculations are floating-point. The vector statement is executed approximately  $n^3/3 + n^2$  times within the inner loop where  $n$  is equal to the matrix order. The inner loop dominates the total execution time.

The standard version of BLAS is written in Fortran; however, assembly coded BLAS can also be

used to optimize for the underlying microprocessor architecture. In addition, the Fortran BLAS comes in two forms: rolled and unrolled. Unrolling means repeating code inside a loop to minimize loop overhead. Usually the BLAS loops are unrolled. However, rolled loops allow the compiler to recognize the vector loops to take advantage of vectorization.

For most systems, the data has to be fetched from external memory due to the need for large amounts of data on the fly. Therefore, not only the floating-point performance, but also the memory subsystem design is evaluated. To take full advantage of the parallel architecture of the i860 microprocessor, one should code the BLAS in assembly code. The capabilities of dual floating point operations (multiplication and addition) per instruction and dual instructions per clock allow the i860 microprocessor to perform the inner loop:  $y[i] = y[i] + a * x[i]$  at high speed. The dual operation instruction allows the arithmetic in the inner loop to complete in one clock. The loading of  $x[i]$  makes use of the pipelined load (PFLD) instruction, which is unique on the i860 microprocessor.  $y[i]$  is obtained from the cache. The final results are pipelined through the adder pipe and stored in memory one result per clock. The data movement and add/multiply instructions are executed in parallel in dual instruction mode.

The vectorized Fortran (rolled) and assembly code (coded) double precision Linpack performance of the i860 microprocessor was measured at 4.5 MFLOPS and 8.7 MFLOPS on the 33.3 MHz board. At 40 MHz, the results were meas-

ured at 5.4 MFLOPS and 10.2 MFLOPS respectively. Since Linpack constantly requires data from external memory, the simple DRAM-only memory design on the measured system results in excess wait states. A high percentage of the memory accesses which could have been zero-wait-state page mode accesses to the DRAM have been found to be starting from idle state in the DRAM state machine. This means that the tested configuration will see eight wait states for reads and five wait states for writes.

Listed in Table 7 are the measured results for the i860 microprocessor and the published data for other microprocessors. The compiled performance of the MIPS R3000 is within 5% of its hand-coded performance. That is a good example of mature software bringing compiled performance close to the inherent performance level of an underlying architecture. Therefore, the vectorized Fortran performance of the i860 microprocessor is expected to approach the assembly coded performance as system software continues to mature.

**Table 7 100x100 Linpack Benchmark Results**

DP Fortran (MFLOPs)	DP Coded (MFLOPs)	Systems
.10		Sun-3/160, 16.7MHz (Rolled BLAS)
.11	-	Sun-260, 25MHz 68020+20MHz 68881 (Rolled BLAS)
.13	.16	DEC MicroVAX II, VAX/VMS
.14	-	Apollo DN4000, 25MHz (68020+68881) [ENEWS 87]
.14	-	VAX 11/780, 4.3BSD. LLL Fortran [ours]
.14	.17	VAX 11/780, VAX/VMS
.20	-	80386+80387, 20MHz, 64K cache, Greenhills
.29	.49	Intergraph IP-32C, 30MHz Clipper [Intergraph 86]
.38	-	80386+Weitek 1167, 20MHz, 64K cache, Greenhills
.41	-	Sun-3/160, Weitek FPA (Rolled BLAS)
.41	.45	DEC Micro VAX 3200/3500/3600, VAX/VMS
.45	.54	HP 9000/840S [HP 87]
.46	-	Sun-3/260, Weitek FPa (Rolled BLAS)
.49	.66	VAX 8600, VAX/VMS 4.5
.49	.54	HP 9000/825S [HP 87]
.57	.72	HP 9000/850S [HP 87]
.60	.72	MIPS M/500, f77 1.21
.65	.76	VAX 8500, VAX/VMS
.70	.96	VAX 8650, VAX/VMS
.78	-	IBM 9370-90, VS FORT 1.3.0
.86	-	Sun-4/110 [Sun 88]
.99	1.2	VAX 8550/8700/8800, VAX/VMS
1.0	1.2	Intel i486 CPU at 25 MHz
1.1	-	Sun-4/200 16.7MHz SPARC (Rolled BLAS) w/Weitek 1164/5 [Sun 87a]
1.2	1.3	MIPS M/800, f77 1.31
1.2	2.2	Motorola 88000, 20MHz, 128K cache [MIPS 89]
1.3	-	Sun SPARCstation 1, SunOS 4.0.3 [Sun 89]
1.5	1.7	ELXSI 6420
1.5	1.6	MIPS M/1000, f77 1.31
1.6	2.0	DECstation 3100, f77 1.31 (Rolled)
1.6	2.0	Alliant FX-1 (1 CE) [Alliant 86]
2.1	-	IBM 3081K H enhanced opt-3
2.1	2.2	MIPS M/120-5, f77 1.31
2.7	-	Sun SPARCsystem 300, SunOS 4.0.3 [Sun 89]
3.0	3.3	CONVEX C-1/XP, Fort 2.0 (Rolled BLAS)
3.6	3.9	MIPS M/2000-8 25MHz R3000/R3010, f77 1.31
3.9	4.1	MIPS M/2000-8 25MHz R3000/R3010, f77 2.0 (Rolled BLAS)
5.1	-	Apollo DN10000 [Apollo 88]
6.0	-	Multiflow Trace 7/200 Fortran 1.4 (Rolled BLAS)
<b>4.5</b>	<b>8.7</b>	<b>Intel i860 <math>\mu</math>P board at 33.3MHz (Fortran vectorized)</b>
<b>5.4</b>	<b>10.2</b>	<b>AL860 Accelerator at 40MHz (Fortran vectorized)</b>
7.6	11.0	Alliant FX-8, 8 CEs, FX Fortran, v2.0.1.9
12.0	23.0	CRAY 1S CFT (Rolled BLAS)
52.0	61.0	ETA10-E (1 proc, 10.5ns)
56.0	60.0	CRAY X--MP/4 CFT (Rolled BLAS)

## *Summary*

The high performance of the i860 microprocessor is made possible by its wide, high speed data bus, high integration and parallel architecture. High integration eliminates signal delay between chips and allows for significant architecture optimization and higher clock frequency. The highly parallel architecture of the i860 microprocessor allows for low instruction clock count design that contributes to its superb vector performance.

As evidenced by the measured data, even a simple i860 microprocessor based system (an add-in board), with a DRAM memory subsystem and no external cache outperforms competitive RISC-based workstations and file-servers currently available in the marketplace. The i860 CPU performance lead will continue to increase as system hardware and software designs mature.

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